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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Brian Doyle

Title: QUANTUM WIRE GATE DEVICE AND METHOD OF MAKING SAME

Docket No.: 884.524US1

Filed: March 1, 2000

Examiner: Neal Berezny

Serial No.: 09/516,653

Due Date: August 21, 2002

Group Art Unit: 2823

BOX AF

Commissioner for Patents
Washington, D.C. 20231

We are transmitting herewith the following attached items (as indicated with an "X"):

- ☒ A return postcard.
- ☒ An Amendment and Response Under 37 CFR 1.116 (7 Pages).
- ☒ Clean Version of Amended Specification Paragraphs (1 pg.).

Please consider this a **PETITION FOR EXTENSION OF TIME** for sufficient number of months to enter these papers and please charge any additional required fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938, Minneapolis, MN 55402 (612-373-6900)

By: Ann M. McCrackin
Atty: Ann M. McCrackin
Reg. No. 42,858

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: BOX AF, Commissioner for Patents, Washington, D.C. 20231, on this 22 day of July, 2002.

Jane E. Brockschink
Name

Jane E. Brockschink
Signature

Customer Number 21186

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
(GENERAL)

P.O. Box 2938, Minneapolis, MN 55402 (612-373-6900)



EXPEDITED PROCEDURE - EXAMINING GROUP 2823

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AMENDMENT & RESPONSE UNDER 37 C.F.R. § 1.116

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PATENT

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#11/C
Amended
J. McInnis
8/2/02

In response to the final Office Action mailed May 21, 2002, please amend the application as follows:

IN THE SPECIFICATION

Please make the paragraph substitutions indicated in the appendix entitled Clean Version of Amended Specification Paragraphs. The specific changes incorporated in the substitute paragraphs are shown in the following marked-up versions of the original paragraphs:

~~Please~~ nb
Enter.
8/6/02

On page 2, beginning at line 16, please amend the paragraph as line follows:

A field effect transistor (FET) is a fundamental building block of integrated circuits. Where metal oxide on silicon [semiconductor] (MOS) devices are approaching the limits of scaling based upon known fundamental technique, optimization of different components has allowed the FET to continue in the process of miniturization. The decrease in supply voltage, however, has caused acceptable performance in the 0.7X scaling to become increasingly elusive. What is needed is a method of achieving gate dimensions that overcome scaling limits of the prior art.